

A Low-Gm Programmable Transconductor Based on FVF Architecture in 180 nm CMOS Process

O. J. Cinco Izquierdo ^{#*1}, J. J. Ocampo Hidalgo ^{&2}, C. A. de la Cruz Blas ⁺³, F. Montalvo Galicia ^{¥4},
M. T. Sanz Pascual ^{§5}

[#] Tecnológico Nacional de México: Instituto Tecnológico José Mario Molina Pasquel y Henríquez
Academic Unit Zapopan, Jalisco, México.

^{*} Intel Tecnologías de México, Zapopan, Jalisco, México.

[&] Electronics Department, Universidad Autónoma de México, México City, México.

⁺ Department of Electrical and Electronic Engineering, Universidad Pública de Navarra, Pamplona,
España.

[¥] Faculty of Basic Sciences, Engineering and Technology, Universidad Autónoma de Tlaxcala,
Tlaxcala, México.

[§] Electronics Department, Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE) Tonantzintla,
Puebla, México.

¹ oscar@zapopan.tecmm.edu.mx, ² jjoh@azc.uam.mx, ³ carlos.aristoteles@unavarra.es, ⁴ mongafre@gmail.com,

⁵ materesa@inaoep.mx

Abstract— This paper presents the design and simulation of a programmable low-transconductance (Gm) operational transconductance amplifier (OTA) suitable for integrated analog filters. The proposed architecture is based on a Flipped Voltage Follower (FVF) core with a source degeneration path implemented using a voltage-controlled MOS pseudo-resistor. This configuration enables wide tunability of the transconductance while maintaining low power consumption and compact area. Designed in a 0.18 μm CMOS process and operating at a 1.8 V supply, the OTA achieves a tunable Gm range from 3.25 nS to 25 nS with a power consumption of only 9 μW . The circuit exhibits a bandwidth of 560 kHz and a total harmonic distortion (THD) below 1% for input signals up to 100 mVpp.

Keywords— Low-Transconductor OTA, Flipped Voltage Follower (FVF), Pseudo-Resistor, Analog Design.

I. INTRODUCTION

Analog signal conditioning plays a critical role in biomedical data acquisition systems, as it enhances signal quality before digital processing. Biomedical signals such as electroencephalograms (EEG), electrocardiograms (ECG), and electromyograms (EMG) exhibit specific characteristics in terms of frequency and amplitude. For instance, EEG signals typically range from 0.5 to 100 Hz with amplitudes in the order of microvolts, while ECG signals span from 0.05 to 150 Hz and can reach amplitudes of several millivolts. These properties demand the implementation of analog filters with low cutoff frequencies to suppress noise and undesired interferences effectively [1-5].

Analog filters can be implemented in CMOS using different techniques, depending on the frequency range, power consumption, and tuning capability. Common alternatives include operational transconductance amplifier

(OTA)-based filters, switched-capacitor (SC), log-domain, and MOSFET-C. In this work, the Gm-C approach is considered because it provides a direct relationship between the filter characteristics and the transconductance of the OTA, while avoiding the need for large passive resistors [6-8]. Since the filter response is strongly affected by process and environmental variations, the ability to adjust G_m provides an additional degree of freedom for compensating these deviations [6-8].

A continuous-time Gm-C filter can be implemented using an integrator as its fundamental building block. The integrator is implemented with a transconductor and a capacitor, shown in Figure 1. The transfer function is expressed as:

$$\frac{V_{out}}{V_{in}} = \frac{G_m}{sC} \quad (1)$$

Therefore, the output voltage is equal to the integration of the differential input voltage multiplied by the unity-gain frequency, which is given by:

$$f_u = \frac{G_m}{2\pi C} \quad (2)$$

Where G_m is the transconductance of the OTA and C is the capacitor value. From (2), a low unity-gain frequency (f_u) can be obtained either by reducing G_m or increasing C. Although using a large capacitor is a straightforward option, the required capacitance can become a significant contributor to the silicon area, particularly at very low frequencies. For this reason, the proposed approach focuses on reducing the transconductance G_m , allowing low-frequency operation.

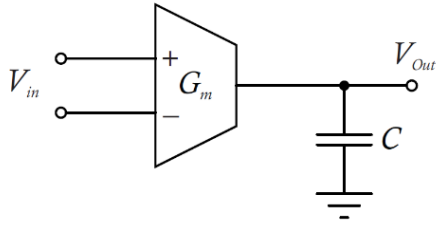


Fig. 1. Single-ended Gm-C Integrator.

This paper presents the design and simulation of a low-transconductance, tunable transconductor circuit that is robust against process variations. Although the design has not been fabricated, extensive simulations have been carried out to validate its performance and its potential for use in analog filtering applications targeting biomedical signals.

The paper is organized as follows. Section II introduces the proposed transconductor along with relevant design considerations. Section III presents the simulation results that validate the performance of the topology. Finally, Section IV summarizes the conclusions of this work.

II. PROPOSED TUNABLE LOW-TRANSCONDUCTANCE OTA

Figure 2 shows the proposed low-transconductance operational transconductance amplifier (OTA), which employs a source-degenerated input stage based on a Flipped Voltage Follower (FVF) topology [9].

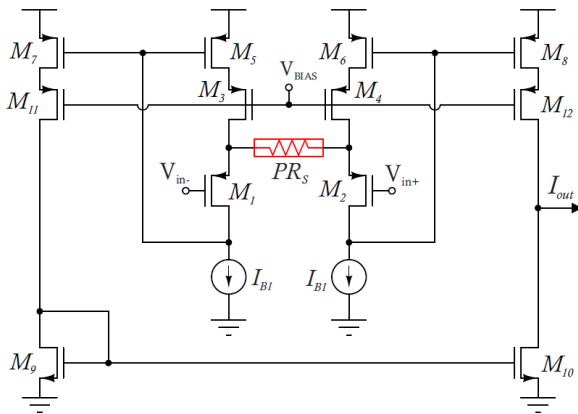


Fig. 2. FVF-based low-Gm OTA proposed.

The differential input pair (M_1 and M_2) receives the signals V_{in-} and V_{in+} and is degenerated by a pseudo-resistor (PRS). The pseudo-resistor enables the implementation of very low effective transconductance G_m and its resistance can be tuned via analog biasing, providing programmability without the need for large passive components.

The FVF structure is composed of transistors M_1 to M_6 . Transistors M_3 and M_4 operate as cascode devices, providing increased output resistance and improving current copying accuracy. Transistors M_5 and M_6 provides shunt feedback, replicate the current from the differential pair and, along with M_7 and M_8 in the output branch, complete the current mirroring path. The degeneration through PRS limits the

current variation with input voltage, effectively defining the OTA's transconductance.

The output current is mirrored through transistors M_5 - M_7 and M_6 - M_8 forming two current mirrors that generate the differential output current I_{out} . Transistors M_9 and M_{10} implement a current mirror that enables single-ended signal extraction, while M_{11} and M_{12} act as cascode devices to enhance output impedance. The common-mode feedback (CMFB) circuit, which is not depicted in the Figure, ensures that the output common-mode level remains within acceptable limits, maintaining differential symmetry and DC stability.

To achieve low transconductance values suitable for low-frequency analog filtering applications, a high-value degeneration resistor (typically in the range of tens to hundreds of megaohms) is required. However, implementing such large resistances with conventional polysilicon resistors would result in a significant increase in chip area, which is undesirable in integrated circuit design.

To address this issue, the proposed transconductor incorporates a MOS-based pseudo-resistor (PRS) instead of a traditional passive resistor. The topology of the PRS is shown in Figure 3, where a series of MOS transistors are connected in such a way that they operate in the subthreshold region, behaving as high-valued nonlinear resistors. The effective resistance can be tuned via the gate voltage V_{TUNE} , allowing programmability of the transconductance G_m .

In the proposed OTA, the PRS is connected between the source nodes of the differential pair to achieve the required degeneration directly within the input stage. Resistance can be adjusted through V_{TUNE} , providing a convenient means of controlling the OTA transconductance without modifying the bias current.

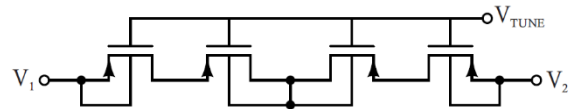


Fig. 3. Pseudo-resistor implementation.

The use of this tunable pseudo-resistor not only ensures area efficiency but also supports ultra-low power operation, as the devices remain in weak inversion. Overall, this approach simplifies the design while providing the flexibility needed for programmable analog signal processing blocks.

A. Small-Signal Analysis of the Transconductor

To understand the behavior of the proposed transconductor and quantify its effective transconductance, a small-signal analysis is performed. The core of the circuit is a differential pair (M_1 and M_2) with a degeneration element implemented using a pseudo-resistor PRS. The Flipped Voltage Follower (FVF) configuration contributes to a low input impedance at the sources of M_1 and M_2 , enabling transconductance control through source degeneration.

Assuming ideal current sources I_{B1} and neglecting channel-length modulation and other second-order effects for

simplicity, the small-signal differential transconductance $G_{m,eq}$ can be derived as follows: Let the differential input be $v_{in} = v_{in+} - v_{in-}$. Due to the symmetrical structure, and assuming matched transistors, the differential current at the output is:

$$i_{out} = g_m(v_{gs1} - v_{gs2}) \cdot 2 \quad (3)$$

However, due to source degeneration via the pseudo-resistor R_{PRS} , the gate-source voltage of M_1 and M_2 is modified. For small signals, the voltage across R_{PRS} is:

$$v_{s1} - v_{s2} = i_d \cdot R_{PRS} \quad (4)$$

Since $i_d = i_{out}/2$, the differential input voltage is approximately:

$$v_{in} = v_{gs1} - v_{gs2} + \frac{i_{out}}{2} \cdot R_{PRS} \quad (5)$$

Solving for i_{out} , we obtain:

$$v_{in} = \frac{i_{out}}{2 \cdot g_m} + \frac{i_{out}}{2} \cdot R_{PRS} = \frac{i_{out}}{2} \left[\frac{1}{g_m} + R_{PRS} \right]$$

$$G_{m,eq} = \frac{i_{out}}{v_{in}} = \frac{2}{\frac{1}{g_m} + R_{PRS}} \approx \frac{2}{R_{PRS}} \text{ if } R_{PRS} \gg \frac{1}{g_m}$$

Thus, for high resistance values R_{PRS} , the equivalent transconductance is dominated by the degeneration resistor and is approximately:

$$G_{m,eq} \approx \frac{2}{R_{PRS}} \quad (6)$$

This result confirms that the effective G_m can be programmed through the control voltage V_{TUNE} , which adjusts the operating region, and hence the resistance, of the MOS transistors forming the pseudo-resistor. This programmability allows the circuit to cover a wide range of G_m values without requiring changes to device dimensions or bias currents.

B. Transistor-Level Sizing

The circuit was designed and sized using a standard 180 nm CMOS technology. The design focuses on achieving a low and tunable transconductance while preserving linearity and minimizing power consumption. Table 1 summarizes the width (W) and length (L) dimensions of all MOSFETs used in the design. The transistor dimensions were selected to meet the matching requirements of the differential pair, provide the required bias conditions for the FVF core, and obtain the desired high resistance in the PRS.

TABLE I

TRANSISTOR SIZE OF PROPOSED TRANSCONDUCTOR

Transistor	$M_{1,2}$	$M_{3,4}$	$M_{5,6}$	$M_{7,8}$	$M_{9,10}$	M_{B1}	M_{B2}
W/L ($\mu m/\mu m$)	528/1	28/1	88/1	132/1	352/1	112/1	352/1

III. SIMULATION RESULTS

A. Nominal Results

The proposed OTA operates from a 1.8 V supply and consumes only 9 μW when biased with a 1 μA reference current. This low-power operation is suitable for energy-constrained applications such as biomedical signal processing. The pseudo-resistor, implemented with PMOS transistors biased in the subthreshold region, enables high resistance values. Either the bulk-drain or bulk-source terminals of the transistors are shorted to improve control and stability. Despite its high resistive behavior, this approach introduces nonlinearity, resulting in increased total harmonic distortion (THD).

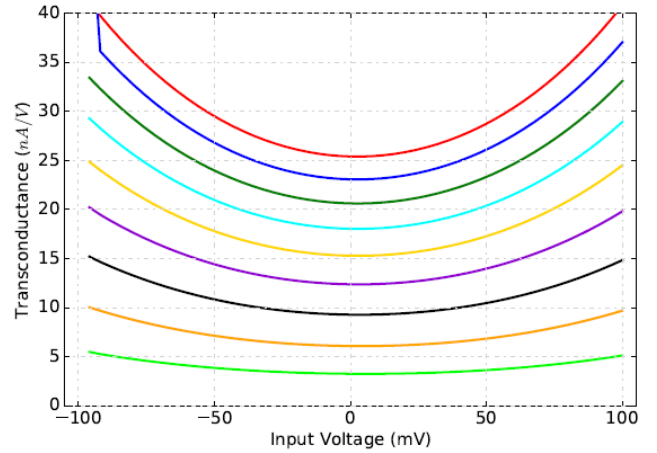


Fig. 4. Dependence of G_m on V_{in} of the transconductor.

By varying the control voltage V_{TUNE} , the equivalent transconductance G_m can be adjusted to compensate for process variations or to tune the cutoff frequency of Gm-C filters. As shown in Figure 4, the OTA achieves a tunable transconductance range from 3.25 nA/V to 25 nA/V as V_{TUNE} is swept from 100 mV to 900 mV. Figure 5 illustrates the dependence of G_m on the input differential voltage, highlighting the inherent nonlinearity of the circuit and its impact on signal distortion.

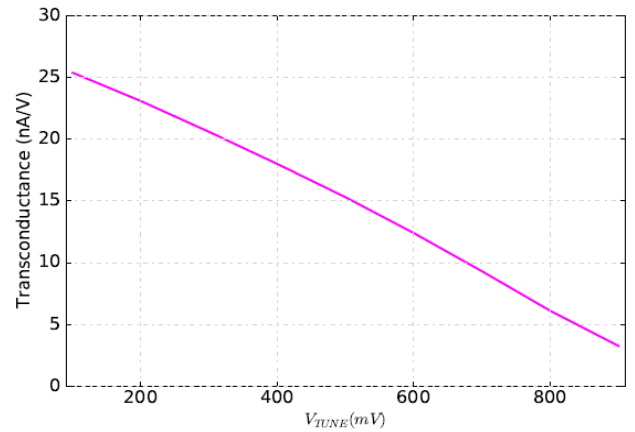


Fig. 5. Transconductance as a function of V_{TUNE} .

Figure 6 shows the total harmonic distortion for a sine differential input voltage at 1 kHz with amplitude varying from 10 mV to 50 mV with $V_{TUNE} = 400\text{mV}$ and a transconductance $G_m = 10\text{nA/V}$. The THD remains below -40dB for input voltages up to 100mV_{pp} . Figure 7 shows the THD when the transconductance changes due to the change in V_{TUNE} , for a sine amplitude voltage of 10mV . In this case, when the transconductance is reduced, the THD increases.

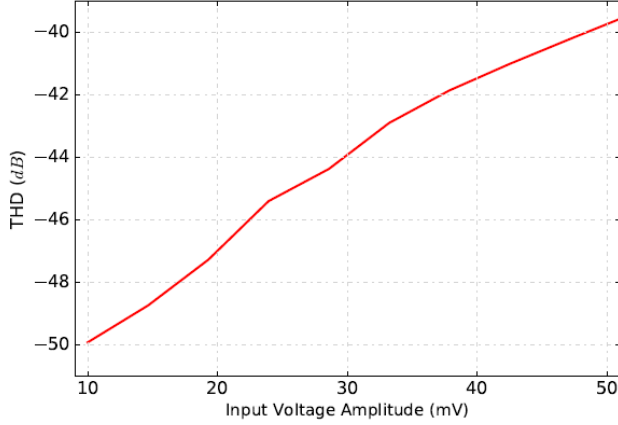


Fig. 6. THD for different input voltage amplitudes.

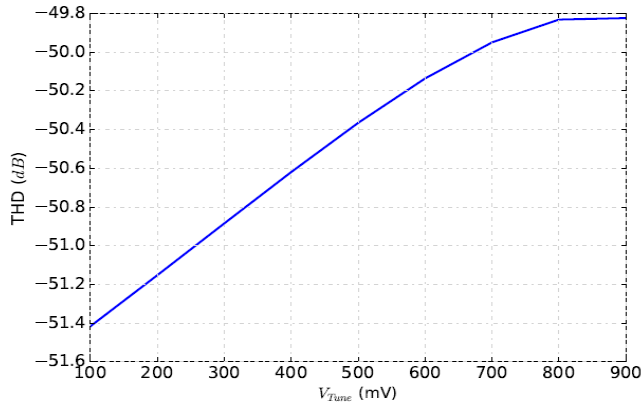


Fig. 7. THD by modifying V_{TUNE} at same input voltage amplitude (10 mV).

Finally, the input-referred power spectral density is as low as $9\text{ }\mu\text{V}/\sqrt{\text{Hz}}$ at 100 Hz.

B. Monte Carlo Analysis

To evaluate the robustness of the proposed tunable low-transconductance OTA against mismatch, a set of 300 Monte Carlo simulations was performed. The first parameter analyzed was the transconductance (G_m), extracted at a DC differential input of 0 V. The histogram shown in Figure 8 reveals a Gaussian distribution centered at a mean value of 3.31 nS, with a standard deviation of 0.63 nS, indicating good robustness of the circuit with limited sensitivity to device mismatch.

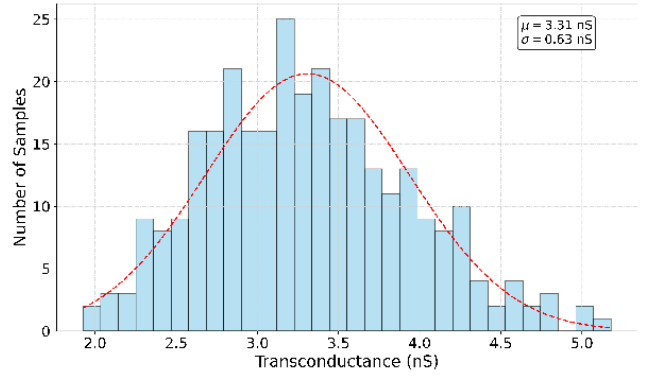


Fig. 8. Monte Carlo Histogram of G_m at $V_{DC} = 0\text{V}$.

The second parameter analyzed was the Total Harmonic Distortion (THD), obtained for a 10 mV differential sinusoidal input at 1 kHz. The corresponding histogram is shown in Figure 9, with a mean THD of -49.97 dB and a standard deviation of 0.32 dB, confirming the linearity and low variability of the circuit under mismatch variations. These results validate the effectiveness of the proposed OTA architecture and the pseudo-resistor biasing technique.

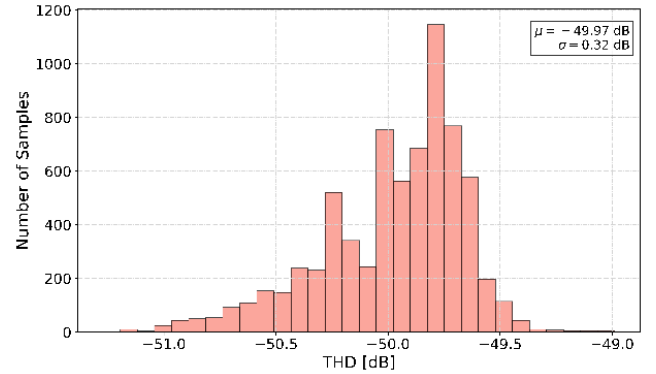


Fig. 9. Monte Carlo Histogram of THD at 10 mVpp Input.

A summary of the key performance metrics obtained through simulation is provided in Table II, where a comparison with recent related works is also included to highlight the advantages of the proposed design.

TABLE II

CHARACTERISTICS OF THE TRANSCONDUCTOR

Parameters	[10]	[11]	This Work
Supply (V)	0.8	1	1.8
G_m (nS)	66	0.62 – 6.2	3.25 – 25
BW (kHz)	0.195	0.1	560
Power (μW)	0.3	0.27	9
THD (%) @ 100 mVpp	1	0.18	1
PSD $\mu\text{V}/\sqrt{\text{Hz}}$	74	-	9 @ 100 Hz

IV. CONCLUSIONS

This work presents a tunable low-transconductance OTA architecture designed in a 0.18 μm CMOS process, optimized for low-power and low-noise applications. The proposed circuit achieves a wide tunability range of the transconductance, from 3.25 nS to 25 nS, through the control voltage V_{TUNE} , enabling flexibility in analog signal processing tasks. The OTA operates with a 1.8 V supply voltage and exhibits an ultra-low power consumption of 9 μW , making it suitable for energy-constrained systems.

The circuit demonstrates a bandwidth of 560 kHz and maintains a THD of 1% at 100 mVpp, ensuring signal integrity for moderate input amplitudes. Monte Carlo simulations validate the robustness of the topology under mismatch conditions, with the transconductance and THD presenting Gaussian distributions centered around 3.31 nS and -49.97 dB, respectively, with low standard deviations. These results, alongside the flexibility provided by the pseudo-resistor configuration, confirm that the proposed OTA is a promising solution for low-frequency, low-power, and high-linearity analog front-ends in biomedical and sensor interface applications.

REFERENCES

- [1] Y. B. Yang, K.C. Chang, and Y.C. Li, "Filtering techniques for extracting bridge frequencies from a test vehicle moving over the bridge," *Engineering Structures*, vol. 48, pp. 353-362, 2013. DOI: <https://doi.org/10.1016/j.engstruct.2012.09.025>.
- [2] Y. Li, C.C.Y. Poon, and Y. Zhang "Analog Integrated Circuits Design for Processing Physiological Signals," *IEEE Reviews in Biomedicak Enginnering*, vol. 3, pp. 93-105, Sep. 2010. DOI: <https://doi.org/10.1109/RBME.2010.2082521>.
- [3] J. Zheng, W. Ki and C. tsui "A Fully Integrated Analog Front End for Biotential Signal Sensing" *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 65, No.11, pp. 3800-3809, 2018. DOI: <https://doi.org/10.1109/TCSI.2018.2854741>.
- [4] M. S. Ansari, "Analog front-end design for biomedical signal acquisition systems," *CSIT*, vol. 7, pp. 199-204, 2019. DOI: <https://doi.org/10.1007/s40012-019-00232-z>.
- [5] V. S. Rajan and B. Venkataramani, "Design of low power, programmable low- G_m OTAs and G_m -C filters for biomedical applications," *Analog Integr Circ Sig Process*, vol. 107, pp. 389-409, 2021. DOI: <https://doi.org/10.1007/s10470-020-01748-0>.
- [6] H. Song. *Design of VLSI Gm-C Filters.* " Chap. 13 in *VLSI Analog Circuits: Algorithms, Architecture, Modeling, and Circuit Implementation*. 2nd ed. New York: McGraw-Hill Education, 2016.
- [7] S.-Y. Lee, C.-P. Wang, and Y.-S. Chu, "Low-voltage OTA-C filter with an area and power-efficient OTA for bio signal sensor applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 13, no. 1, pp. 56-67, 2018. DOI: <https://doi.org/10.1109/TBCAS.2018.2882521>.
- [8] O. J. Cinco Izquierdo, C. A. De la Cruz Blas, M. T. Sanz Pascual, J. J. Ocampo Hidalgo, "Tunable Low Frequency G_m -C Low-Pass Filter using an OTA with Bootstrapping," *Circuits Syst Signal Process*, vol. 44, pp. 1443-1455, 2025. <https://doi.org/10.1007/s00034-024-02897-7>.
- [9] R. G. Carvajal, J. Ramirez Angulo, A. J. Lopez Martin, A. Torralba, J. A. G. Galan, A. Carlosena, and F. M. Chavero, "The flipped voltage follower: a useful cell for low-voltage low-power circuit design," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 7, pp. 1276-1291, 2005. DOI: <https://doi.org/10.1109/TCSI.2005.851387>.
- [10] P. R. Agostinho, S. A. P. Haddad, J. De Lima, and W. A. Serdijn "An ultra low power CMOS pA/V transconductor and its application to wavelet filters," *Analog Integr Circ Sig Process*, vol. 57, pp. 19-27, 2008. DOI: <https://doi.org/10.1007/s10470-008-9193-6>.
- [11] J. Jakusz, W. Jendernalik, G. Blakiewicz, M. Kłosowski, and S. Szczepański, "A 1-nS 1-V Sub-1- μW Linear CMOS OTA with Rail-to-Rail Input for Hz-Band Sensory Interfaces," *Sensors*, vol. 20, no. 11, pp. 3303, 2020. DOI: <https://doi.org/10.3390/s20113303>.